

PATENT

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ABSTRACT OF THE DISCLOSURE

A Viterbi decoder is described, having a calculation unit (ACSU) for a Radix- 2^x trellis which, for each trellis state, adds the respectively associated 2^x branch metrics (ZMi) to the already accumulated 2^x path metrics (PMM) from 2^x predecessor trellis states, and selects those of the 2^x path metrics (PMi) which have been determined in this way to be extreme as the new accumulated path metric (PMM) for the addition process in the next period, with said calculation unit containing:

for each trellis state, 2^x parallel cascades of processor elements (PE) for pipeline processing of the bits in the branch metrics and in the path metrics (PMM) and, for each trellis state, in each case one extreme value selection device (MAX) for all the processor elements of the same order (q) within the pipeline. According to the invention, the number of processor elements (PE) in each of the cascades is less than the number m of the bits which are used for the binary number representation of the value range of the path metrics (PM). For this purpose, process or elements in each cascade are designed such that they in each case process disjunct groups of $p \geq 2$ bits cohesively.